This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. – 2. (Canceled)

3. (Currently Amended) A ~~The~~ method of providing error correction in an integrated circuit (IC) to enable the replacement of a defective logic function implemented within the IC, the method comprising: ~~of claim 2,~~

providing an embedded field programmable gate array (FPGA) in the IC to perform logic error correction;

providing registers and associated circuitry designed to manipulate a scanned data stream;

identifying a defective logic function within the IC;

programming the embedded FPGA to replace the defective logic function;

identifying all inputs in an input cone of logic of the defective logic function;

directing all inputs in the input cone of logic of the defective logic function into the embedded FPGA, such that the embedded FPGA replaces the defective logic function with an error corrected version of the defective logic function, wherein said directing of all inputs in the input cone of logic of the defective logic function into the embedded FPGA includes:

placing a logic macro implemented in the IC into a wait state; and

scanning data from the defective logic function into the FPGA and the registers and associated circuitry to implement error correction of the defective logic function; and,

identifying all outputs in an output cone of logic of the defective logic function;

directing an output of the FPGA to the output cone of logic of the defective logic function, such that logic error correction is provided within the embedded FPGA structure of the IC.

wherein a scan chain defines a data path through the IC, and a feedback loop is formed to direct corrected data of the scan chain to a register boundary of the defective logic function, whereupon the logic macro discontinues the wait state and resumes normal processing.

4. (Currently Amended) The method of claim [[1]] 3, wherein a scan chain defines a data path through the IC, and corrected data of the scan chain is scanned back around, upstream or downstream, to an origin of the corrected data.

5. (Currently Amended) The method of claim [[1]] 3, wherein a plurality of said embedded FPGAs are ~~strategically placed throughout the design of the~~ operatively connected for receiving scan chain data from one or more logic functions within an IC.

6. (Currently Amended) The method of claim [[1]] 3, wherein a plurality of scan chains define a plurality of data paths through the IC, and a plurality of said embedded FPGAs being operatively connected for receiving said scan chain data from one more logic functions within said IC ~~are strategically placed throughout the design of the logic function IC~~ to correct data in the plurality of scan chains.

7. (Currently Amended) The method of claim [[1]] 3, wherein a plurality of scan chains define a plurality of data paths through the IC, and data to be corrected in the plurality of scan chains are multiplexed into a single dedicated FPGA that is time multiplexed between the plurality of scan chains.

8. (Currently Amended) The method of claim [[1]] 3, wherein a plurality of scan chains define a plurality of data paths through the IC, and data to be corrected in the plurality of scan chains are multiplexed into a single FPGA that is time multiplexed between the plurality of scan chains and also with normal system functions performed by the single FPGA.

9. (Currently Amended) The method of claim [[1]] 3, further including:

identifying defective logic functions of the IC;

tracing a cone of logic of each identified defective logic function forward and

backward to register boundaries; and,

~~identifying a plurality of correction solutions, such as correcting bad data bits, correcting upstream data, correcting downstream data;~~

selecting and implementing a ~~one or more of the~~ correction ~~solutions~~ solution comprising one or more of: correcting bad data bits, correcting upstream data, or correcting downstream data.

10. (Currently Amended) The method of claim [[1]] 3, further including:

identifying defective logic functions in a logic macro implemented in the IC;

analyzing dataflow through the IC with respect to each identified defective logic function; and

identifying an optimum stage in the IC logic macro for which a logic breakpoint may be inserted to enable replacement of a defective logic function of said identified defective logic functions.

11. (Original) The method of claim 10, wherein the logic breakpoint is set by a comparison of a program count of a program counter for the IC with a preselected count of the program counter.

12. (Original) The method of claim 10, wherein the logic breakpoint is set based upon a preselected number of clock cycles of a clock of the IC.

13. (Currently Amended) The method of claim [[1]] 3, further including:

identifying defective logic functions in a logic macro implemented in the IC;

analyzing dataflow through the IC with respect to each identified defective logic function; and

identifying an optimum point in a timing path of a defective logic function to insert a logic breakpoint to enable replacement of the defective logic function.

14. (Original) The method of claim 13, wherein the logic breakpoint is set by a comparison of a program count of a program counter for the IC with a preselected count of the program

counter.

15. (Original) The method of claim 13, wherein the logic breakpoint is set based upon a preselected number of clock cycles of a clock of the IC.

16. (Currently Amended) The method of claim [[1]] 3, further including extracting register transfer language (RTL), identifying and implementing RTL updates that are required and feasible.

17. (Currently Amended) The method of claim [[1]] 3, wherein a plurality of scan chains define a plurality of data paths through the IC, and including using separate scan chain clocks and a separate FPGA clock to advance the data of one scan chain at a time independently of other scan chains and the FPGA.

18. (Currently Amended) The method of claim [[1]] 3, wherein the FPGA includes an input correction register and an output correction register, and further including storing a program in a RAM to program which bits of a scan chain data stream are used to set the input correction register of the FPGA, and which bits of the scan chain data stream are replaced with bits from the output correction register of the FPGA.

19. (Currently Amended) The method of claim 18, wherein a bit mapping generated from the scan chain data stream corresponding to a stream of data output from the defective logic function passes through the input correction register, ~~an incoming~~ said scan chain data stream [[is]] being captured in input latches of the input correction register if a program count of a program counter of the IC matches a preselected count.

20. (Currently Amended) The method of claim [[1]] 3, further including providing a multiplexer at an output of the FPGA, and if a program count of a program counter of the IC matches a preselected count, using the multiplexer to replace bit(s) of a scan chain bit stream with bit(s) at the output of the FPGA.

21. (Withdrawn) The method of claim 1, applied in evaluating error recovery of the IC chip design, wherein data errors are injected through the embedded FPGA into the IC chip, and then the logic function IC design is evaluated as to how well it handles error recovery.

22. (Withdrawn) An integrated circuit (IC) with logic error detection and correction capability adapted for use with an in-circuit emulator device for logic breakpoint analysis, the IC comprising:

a system logic function, such as a microprocessor;

an embedded field programmable gate array (FPGA) adapted to implement logic error correction (EC) to the system logic function;

a plurality of scan chain data paths in the IC enabling transfer of data from a plurality of latch circuits at predetermined points in a plurality of logic paths of the system logic function;

a controller to facilitate transfer of data and control signals between the system logic function and the embedded FPGA and to determine a plurality of logic breakpoints in the system logic function;

a plurality of separate clocks provided for the system logic function, the FPGA, and for each scan chain data path.

23. (Withdrawn) The IC of claim 22, further including a plurality of said embedded FPGAs strategically placed throughout the IC.

24. (Withdrawn) The IC of claim 22, wherein a plurality of scan chains define a plurality of data paths through the IC, and a plurality of said embedded FPGAs are strategically placed throughout the IC to correct data in the plurality of scan chains.

25. (Withdrawn) An integrated circuit (IC) with logic error detection and correction capability adapted for use with an in-circuit emulator device for logic breakpoint analysis, the IC comprising:

an embedded field programmable gate array (FPGA) adapted to implement logic repairs to the IC;

a plurality of scan chains data paths in the IC enabling transfer of data from a plurality of latch circuits at predetermined points in a plurality of logic paths in the IC;

a controller to facilitate transfer of data and control signals between the IC and the embedded FPGA and to determine a plurality of logic breakpoints in the IC;

a first clock for the IC,

a second clock for the FPGA;

a third clock for the controller;

a random access memory (RAM) and memory controller to store scan chain programming information;

at least one correction register for storing scan chain correction data to be added to one of the plurality of scan chains.

26. (Withdrawn) The IC of claim 25, further including a plurality of said embedded FPGAs strategically placed throughout the IC.

27. (Withdrawn) The IC of claim 25, wherein a plurality of scan chains define a plurality of data paths through the IC, and a plurality of said embedded FPGAs are strategically placed throughout the IC to correct data in the plurality of scan chains.

28. – 29. (Canceled)

30. (Currently Amended) A ~~The~~ method of debugging and repairing logic errors of an integrated circuit (IC) performing a logic function, and having a system clock, the method comprising the steps of:

~~of claim 28,~~

incorporating a scan chain function circuit in the IC;

setting a plurality of logic breakpoints in the logic function;

detecting a logic error in the IC;

cycling a scan chain data path through the IC and capturing an input data stream of the scan data path in a set of latches feeding an embedded field programmable gate array (FPGA);

initiating a waiting state of the IC logic function while a logic function error correction is identified and implemented by the embedded FPGA within a single clock cycle of a system clock for the IC;

repeating the cycling a scan chain data path by feeding said input data stream of the scan data path to the embedded FPGA with a repaired logic function; and

resuming normal execution and clocking of the IC logic function.

wherein ~~including defining~~ a plurality of scan chain data paths are provided through the IC, and ~~strategically placing a plurality of~~ with one or more said embedded FPGAs being operatively connected for receiving respective scan chain data from one more logic functions throughout the IC to correct data in the plurality of scan ~~chains~~ data paths.